

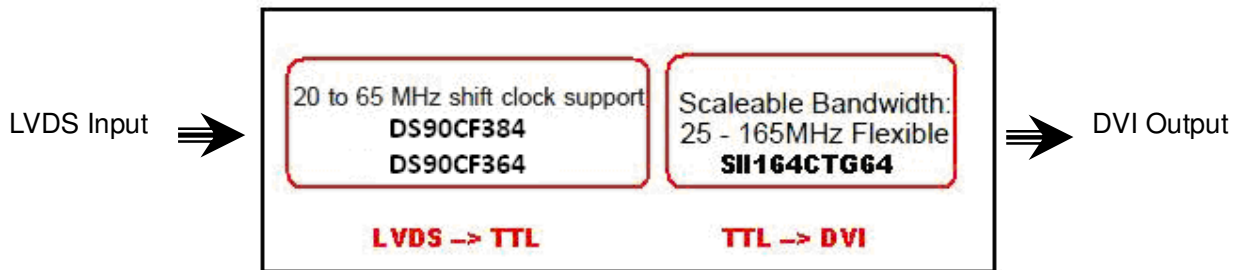
FAQ / Application Note

Subject : Hardware limitation of EPM-1522 hardware A version	
FAQ Document No: G13006	Date: 2013/04/19
Model Name. EPM-1522 A	Rev. A1
Category: <input checked="" type="checkbox"/> General <input checked="" type="checkbox"/> H/W <input type="checkbox"/> S/W <input type="checkbox"/> Others, <u>Specification</u>	
Purpose : EPM-1522 is an 18/24 bit LVDS to DVI transistor. It only supports 20 ~ 65 MHz shift clock input.	

EPM-1522 A1 has two Versions.

EPM-1522-18-A1R supports 18bit LVDS by DS90CF364, EPM-1522-24-A1R supports 24bit LVDS by DS90CD384.

Hardware design of EPM-1522



Because the max clock frequency on DS90CF364/ DS90CF384 (LVDS Receiver) is 65MHz, no matter what LVDS panel and resolutions you select, the clock frequency that offers to EPM-1522 should be lower than 65MHz.

$$60\text{Hz} * \text{Vertical Total} * \text{Horizontal Total} = \text{Shift Clock Frequency} \leq 65\text{MHz}$$

Vertical Total = Vertical Blank + Vertical Display Period

Horizontal Total = Horizontal Blank + Horizontal Display Period

According to the above formula, you could calculate and get the Shift Clock Frequency easily.

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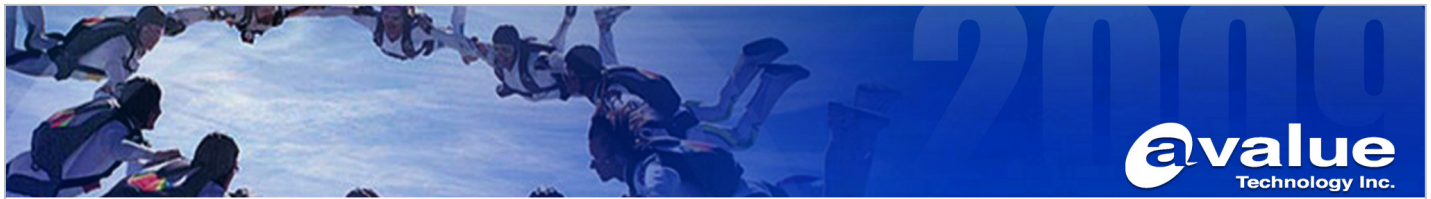
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For example:

VESA Monitor Timing Standard 1024x768 at 60Hz

$$1344 \times 806 \times 60 = 64.99 \text{ MHz}$$

The shift clock (Pixel Clock) on this resolution is around 65MHz under EPM-1522 spec.

If the resolution becomes 1024x768 at 70Hz, the shift clock frequency would be 75MHz which is over chipset's spec. and can't be used with EPM-1522.

VESA MONITOR TIMING STANDARD

Adopted: 9/10/91 (VESA #901101A)
 Resolution: 1024 x 768 at 60 Hz (non-interlaced)
 EDID ID: DMT ID: 10h; STD 2 Byte Code: (61, 40)h; CVT 3 Byte Code: n/a
 BIOS Modes: 104h, 105h, 116h, 117h, & 118h (4, 8, 15, 16, & 24 bpp)
 Method: ***** NOT CVT COMPLIANT *****

Detailed Timing Parameters

Timing Name	= 1024 x 768 @ 60Hz;		
Hor Pixels	= 1024;	// Pixels	
Ver Pixels	= 768;	// Lines	
Hor Frequency	= 48.363;	// kHz	= 20.7 usec / line
Ver Frequency	= 60.004;	// Hz	= 16.7 msec / frame
Pixel Clock	= 65.000;	// MHz	= 15.4 nsec ± 0.5%
Character Width	= 8;	// Pixels	= 123.1 nsec
Scan Type	= NONINTERLACED;	// HPhase =	5.1 %
Hor Sync Polarity	= NEGATIVE;	// HBlank =	23.8% of HTotal
Ver Sync Polarity	= NEGATIVE;	// VBlank =	4.7% of VTtotal
Hor Total Time	= 20.677;	// (usec)	= 168 chars = 1344 Pixels
Hor Addr Time	= 15.754;	// (usec)	= 128 chars = 1024 Pixels
Hor Blank Start	= 15.754;	// (usec)	= 128 chars = 1024 Pixels
Hor Blank Time	= 4.923;	// (usec)	= 40 chars = 320 Pixels
Hor Sync Start	= 16.123;	// (usec)	= 131 chars = 1048 Pixels
// H Right Border	= 0.000;	// (usec)	= 0 chars = 0 Pixels
// H Front Porch	= 0.369;	// (usec)	= 3 chars = 24 Pixels
Hor Sync Time	= 2.092;	// (usec)	= 17 chars = 136 Pixels
// H Back Porch	= 2.462;	// (usec)	= 20 chars = 160 Pixels
// H Left Border	= 0.000;	// (usec)	= 0 chars = 0 Pixels
Ver Total Time	= 16.666;	// (msec)	= 806 lines HT - (1.06xHA)
Ver Addr Time	= 15.880;	// (msec)	= 768 lines = 3.98
Ver Blank Start	= 15.880;	// (msec)	= 768 lines
Ver Blank Time	= 0.786;	// (msec)	= 38 lines
Ver Sync Start	= 15.942;	// (msec)	= 771 lines
// V Bottom Border	= 0.000;	// (msec)	= 0 lines
// V Front Porch	= 0.062;	// (msec)	= 3 lines
Ver Sync Time	= 0.124;	// (msec)	= 6 lines
// V Back Porch	= 0.600;	// (msec)	= 29 lines
// V Top Border	= 0.000;	// (msec)	= 0 lines

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